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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,167	12/02/2008	Ralf Wirth	12406-212US1 5063 P2004,0150 U	
	7590 07/25/201 ARDSON P.C. (SV)	1	EXAMINER	
PO BOX 1022			WOLDEGEORGIS, ERMIAS T	
MINNEAPOLI	S, MN 55440-1022		ART UNIT	PAPER NUMBER
			2893	
			NOTIFICATION DATE	DELIVERY MODE
			07/25/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

	Application No.	Applicant(s)				
Office Astion Comments	10/588,167	WIRTH ET AL.				
Office Action Summary	Examiner	Art Unit				
	ERMIAS WOLDEGEORGIS	2893				
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the c	orrespondence ad	ldress			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DOWN THE MAILING DOWN THE SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period to Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be timused and will expire SIX (6) MONTHS from a cause the application to become ABANDONE!	l. ely filed the mailing date of this c (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 13 M	lav 2011.					
	action is non-final.					
/ <u> </u>		secution as to the	merits is			
	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
	expans Guayie, 1000 G.B. 11, 10	0.0.210.				
Disposition of Claims						
 4) ☐ Claim(s) 1-59 is/are pending in the application. 4a) Of the above claim(s) 21-58 is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-20 and 59 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/o 	vn from consideration.					
Application Papers						
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acc Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex	epted or b) objected to by the Eddrawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	37 CFR 1.85(a). ected to. See 37 Cl	, ,			
Priority under 35 U.S.C. § 119						
a) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list	s have been received. s have been received in Application rity documents have been receive J (PCT Rule 17.2(a)).	on No ed in this National	Stage			
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No (S)/Mail Date 3/30/2010 5/02/2005	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ite				

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DETAILED ACTION

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1. Election/Restrictions

Applicant's election without traverse of invention Group I (claims 1-20 and 59) in the reply filed on 05/13/2011 is acknowledged.

Claims 21-58 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 05/13/2011.

2. Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

3. Information Disclosure Statement

The information disclosure statements filed on 09/30/2010 and 08/02/2006 has been acknowledged and signed copies of the PTO-1449 are attached herein.

4. Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 17 recites the limitation "said envelope" in line 2. There is insufficient antecedent basis for this limitation in the claim.

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5. Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 6. Claims 1-8, 13-16 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kohno et al. (WO 03044872, hereinafter "Kohno"; its US equivalent PG. Pub. 2005/0012109 A1 is used for rejection).

In regards to claim 1, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) an optoelectronic component comprising a semiconductor function region (4) with an active zone (15) and a lateral main direction of extension (D100), wherein said semiconductor function region (4) is provided with at least one opening (10) through said active zone (15), and disposed in the region of said opening (10) is a connecting conductor material (31) that is electrically isolated from said active zone (15) at least in a subregion of said opening.

In regards to claim 2, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) an optoelectronic component comprising a semiconductor function region (4) with an active zone (15) and a lateral main direction of extension (D100), wherein said semiconductor function region (4) is provided with a lateral side face (100) bounding said active zone (15), and disposed

after said side face(100) in the lateral direction is a connecting conductor material (31) that is electrically isolated from said active zone (15) at least in a subregion of said side face (100).

In regards to claim 3, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said connecting conductor material (31) is at least partially electrically isolated from said active zone (15) by an isolation material (102).

In regards to claim 4, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said opening (10) is configured as a depression in the lateral direction (D100) or said side face (100) is provided with a depression in the lateral direction (D100).

In regards to claim 5, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said isolation material (102) at least partially lines said opening (10+2).

In regards to claim 6, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said opening (10) extends in the vertical direction (D200) all the way through said semiconductor function region (4).

In regards to claim 7, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said semiconductor function region (4) comprises a first main face (99) and a second main face (99') located oppositely from said first main face (99) relative to said active zone (15), and said

semiconductor function region (4) is connected electrically conductively to said connecting conductor material (31) on the side comprising said first main face (99).

In regards to claim 8, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said connecting conductor material (31) is electrically isolated from said second main face (99') of said semiconductor function region (4).

In regards to claim 13, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said semiconductor function region (4) is disposed on a carrier (11).

In regards to claim 14, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said connecting conductor material (31) extends to a side of said carrier (11) that is opposite said semiconductor function region (4).

In regards to claim 15, Kohno discloses (Par [0071]) said component (1) can be fabricated in the wafer composite.

In regards to claim 16, Kohno discloses (**Par** [0071])said semiconductor function regions (4) are disposed at least partially side by side in the lateral direction.

In regards to claim 20, Kohno discloses (**Par [0071]**) said device (**1**) can be fabricated in the wafer composite.

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7. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohno.

In regards to claim 9, Kohno discloses (Fig. 3, See annotated and attached Fig. 3 below) said opening (10) but fails to explicitly teach that the lateral dimension of said opening is equal to 100 µm, or less.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984);

In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). Furthermore, the specification contains no disclosure of either the critical nature of the claimed thickness range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Finally, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the lateral dimension of the opening 100µm or less since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

9. Claims 10-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohno in view of Oshio et al. (US 2001/0042865 A1, hereinafter "Oshio").

In regards to claims 10 and 11, Kohno discloses all limitations of claim 1 above but fails to explicitly teach an envelope forms at least partially around said semiconductor function region (claim 10); and said envelope is transparent to a radiation to be generated or received by said active zone (claim 11).

Oshio while disclosing a semiconductor light emitting device (abstract) teaches (Fig. 1) an envelope (5) forms at least partially around said semiconductor function region (1) (claim 10);

said envelope (5) is transparent (Par [0046]) to a radiation to be generated or received by said active zone (1)(claim 11).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the envelop and encapsulation of Oshio into Kohno because as taught by Oshio in Par [0051], having the encapsulation and envelope resins would help improve humidity resistance of the device; and decrease thermal stress-cracking. Furthermore, according to Oshio Par [0070], having the encapsulation would converge the light emitted from the light emitting element to improve the luminance remarkably.

In regards to claim 12, Kohno discloses all limitations of claim 1 above but fails to explicitly teach said active zone is surrounded by an encapsulation that is substantially hermetically tight.

Oshio discloses (Fig. 1) said active zone (1) is surrounded by an encapsulation (9) that is substantially hermetically tight.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the envelop and encapsulation of Oshio into Kohno because as taught by Oshio in Par [0051], having the encapsulation and envelope resins would help improve humidity resistance of the device; and decrease thermal stress-cracking. Furthermore, according to Oshio Par [0070], having the encapsulation would help converge the light emitted from the light emitting element to improve the luminance remarkably.

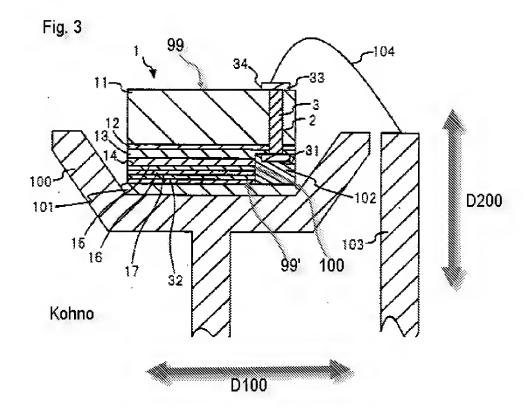
In regards to claims 17-19, Kohno discloses all limitations of claim 16 above but fails to explicitly teach said envelope is configured in one piece and at least partially forms around said semiconductor function regions (claim 17); said semiconductor function regions are mechanically stabilized by a stabilization layer (claim 18); and said envelope is configured as a stabilization layer or part of said stabilization layer (claim 19).

Oshio discloses (Fig. 1) said envelope (5) is configured in one piece and at least partially forms around said semiconductor function regions (1); said semiconductor function regions (1) are mechanically stabilized by a stabilization layer (5+10A); and said envelope (5) is configured as a stabilization layer or part of said stabilization layer (5+10A).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the envelop and encapsulation of Oshio into Kohno because as taught by Oshio in Par [0051], having the encapsulation and envelope resins would help improve humidity resistance of the device; and decrease thermal stress-cracking.

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10. Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is (571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/ Examiner, Art Unit 2893